



EM7-2300

Secure Magnetic Card Reader IC

Feature

- 1.7V to 3.6V Operating Voltage.
- ISO 7811/7812/7813 Compliant.
- Triple-Track Magnetic Stripe Head Interface.
- Acceptable amplitude from 10% to 155% of ISO reference voltage.
- Fast Wipe NV SRAM for Key Storage
- AES Encryption (128/192/256 Bit)
- DES/TDEA Algorithm Support
- Random-Number Generator Hardware
- Self-Destruct Input for Tamper Detection
- Supply Overvoltage Detection
- Low-Power Operation.
- SPI or I²C interface.
- 6MHz Internal Oscillator (±10%).

Description

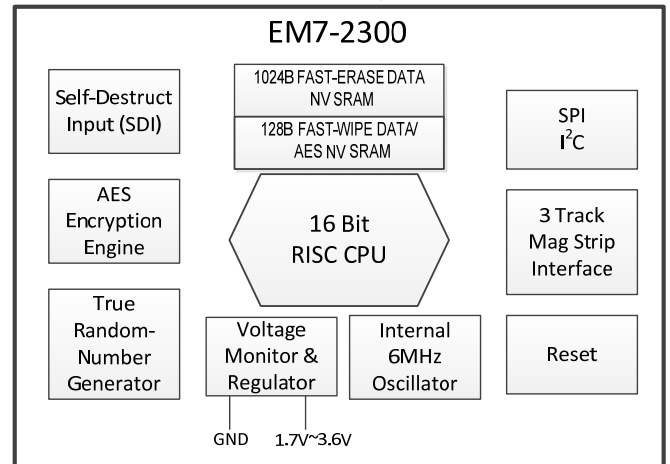
Secure Magnetic Card Reader (EM7-2300) is an integrated triple-track magnetic stripe reader IC that adds security features. Card data can be encrypted using either AES or DES/TDES algorithms. Security is further enhanced with the inclusion of fast-wipe nonvolatile SRAM (NV SRAM), a hardware random number generator (RNG), voltage attack sensors, and a self-destruct input pin. The NV SRAM clears its contents when a tamper is detected by the on chip tamper detection circuitry.

The fast-wipe feature ensures that any data in the NV SRAM is destroyed before any application software can access it. The EM7-2300 communicates to a host processor through an SPI or I²C interface.

Applications

- Magnetic stripe card reader
- ATM/Financial Terminals
- POS
- Security Control

Functional block diagram



Ordering information

No	Interface	Part Number
1	SPI / I ² C	EM7-2300

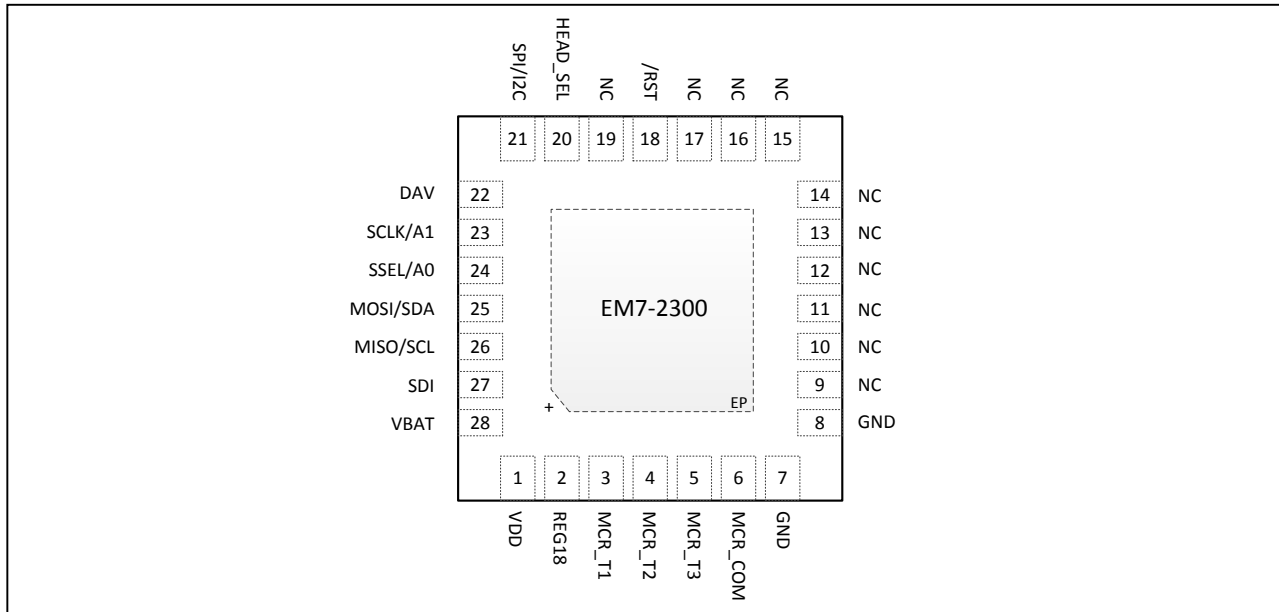
Coded character

Item		Content		
ISO 7811 ~ 7813	Track	Track 1	Track 2	Track 3
	Recording Density	210 BPI	75 BPI	210 BPI
	Capacity	79 Characters (7 Bit Code)	40 Characters (5 Bit Code)	107 Characters (5 Bit Code)
	Start / End Code	% / ?	; / ?	; / ?

EM7-2300

Secure Magnetic Card Reader IC

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
POWER PINS		
1	V _{DD}	Digital Supply Voltage
2	REG18	Regulator Capacitor. This pin must be connected to ground through an external 1μF external ceramic chip capacitor. This capacitor should be placed as close to this pin as possible.
7	GND	Digital Ground
8	GND	Digital Ground
28	VBAT	Battery Supply Voltage
RESET PIN		
18	/RST	Active-Low Reset. This bidirectional pin serves as the active low external reset. When an external low pulse of more than 400μs is recognized, the device will assert and hold an internal reset as long as the pin is held low. It also acts as an output when the source of the reset is internal to the device (e.g., power-fail). In this case, the pin is low as long as the processor is in the reset state.
SELF-DESTRUCT PIN		
27	SDI	Self-Destruct Input. This pin can trigger a security response to external events when connected with external tamper-detection circuitry. The pin contains filter circuits and can be configured as normally open or normally closed independently for specific applications. Activation destroys internal sensitive data. In normally open mode, this pin has an internal pulldown to GND.



EM7-2300

Secure Magnetic Card Reader IC

PIN	NAME	FUNCTION		
PROGRAMMING/CONFIGURATION INTERFACE PINS				
These pins are the programming and configuration interface for the device. Unconnected pins read as a logic 1.				
20	HEAD_SEL	Head Inductance Select Default. HEAD_SEL = 1: Low inductance (20mH~60mH). HEAD_SEL = 0: High inductance (80mH~140mH).		
21	SPI/I2C	SPI or I ² C Communication Interface. SPI/I2C = 1: Select SPI Mode. SPI/I2C = 0: Select I ² C Mode.		
22	DAV	Data available output.		
23	SCLK/A1	SPI/I2C = 1	SPI/I2C = 0	
		SPI Slave Clock Input	I ² C Slave Address A[1:0] Default. The least-significant bit is ignored when comparing addresses.	
24	SSEL/A0	SPI Slave Select Input	A[1:0]	Slave Address
			00	0101_000x
			01	0101_001x
			10	0101_010x
			11	0101_011x
25	MOSI/SDA	SPI Master Out, Slave In Input	I ² C SDA	
26	MISO/SCL	SPI Master In, Slave Out Output	I ² C SCL	
MAGNETIC STRIPE READER PINS				
3	MCR_T1	Magnetic Stripe Reader Track 1 Signal. This analog input should be connected to the magnetic stripe reader associated with track 1. This pin must be connected to MCR_COM if not used.		
4	MCR_T2	Magnetic Stripe Reader Track 2 Signal. This analog input should be connected to the magnetic stripe reader associated with track 2. This pin must be connected to MCR_COM if not used.		
5	MCR_T3	Magnetic Stripe Reader Track 3 Signal. This analog input should be connected to the magnetic stripe reader associated with track 3. This pin must be connected to MCR_COM if not used.		
6	MCR_COM	Magnetic Stripe Reader Common Node. This pin is the common node for all three track signal inputs.		
NC PINS				
9-17,19	NC	Reserved for Future Use. Do not connect this pin.		
EXPOSED PAD				
—	EP	Exposed Pad. Connected to GND.		



EM7-2300

Secure Magnetic Card Reader IC

Absolute Maximum Ratings

(All voltages with respect to GND.)

Voltage Range on V_{DD}-0.3V to +3.6V
 Voltage Range on Any Lead.....-0.3V to ($V_{DD} + 0.5V$)
 Continuous Output Current
 Any Single I/O Pin.....25mA
 All I/O Pins Combined.....25mA

Operating Temperature Range.....-40°C to +85°C
 Storage Temperature Range.....-65°C to +150°C
 Lead Temperature (soldering, 10s).....+300°C
 Soldering Temperature (reflow).....+260°C

Electrical Characteristics

(Limits are 100% tested at $T_A = +25^\circ C$ and $T_A = +85^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	Do not execute the lock or unlock commands if $V_{DD} < 1.85V$	V_{RST}		3.6	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD} (Note 1)	1.64	1.67	1.7	V
Power-On-Reset Voltage	V_{POR}	Monitors V_{DD}		1.6		V
Battery Supply Voltage	V_{BAT}		2.4		3.6	V
Battery-On Reset Voltage (Low-Battery Attack Sensor Threshold)	V_{BOR}	V_{DD} must drop to 0V, then rise			1.6	V
Supply Current	I_{DD}	Measured on V_{DD} pin, device not in reset, all inputs connected to GND or V_{DD} ; outputs do not source/sink any current; not including MCR AFE current (ITRACK)		1.5	2.0	mA
DIGITAL I/O (SDI, SPI, I²C, DAV, RST)						
Input High Voltage (MOSI, SSEL, SDA, SCL, /RST, SDI)	V_{IH}		$0.7 \times V_{DD}$		V_{DD}	V
Input Hysteresis	V_{IHYS}	GBD		300		mV
Input Low Voltage (MOSI, SSEL, SDA, SCL, /RST)	V_{IL1}		V_{GND}	$\frac{1}{2} \times V_{DD}$		V
Input Low Voltage (SDI)	V_{IL2}		V_{GND}	$\frac{1}{2} \times V_{DD}$		V
Output Low Voltage (MISO, DAV, SDA, SCL, /RST)	V_{OL}	$V_{DD} = 2.4V, I_{OL} = 4mA$	V_{GND}		0.5	V
Output High Voltage (MISO, DAV, SDA, SCL, /RST)	V_{OH}	$V_{DD} = 2.4V, I_{OH} = -2mA$	$V_{DD} - 0.5$		V_{DD}	V
Input Leakage Current	I_L	Internal pullup disabled	-100		+100	nA
Input Pullup Resistance Low Voltage (MOSI, SSEL, SDA, SCL, /RST)	R_{PU}			28		k Ω



EM7-2300

Secure Magnetic Card Reader IC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SELF-DESTRUCT INPUT PIN (SDI)						
Pullup Resistance (SDI)	R _{UP}	Normally-closed mode, pulsed voltage source: 500ms period, driven 100µs per period (approximately)	20	40	55	kΩ
Pulldown Resistance (SDI)	R _{DN}	Normally-open mode	20	40	55	kΩ
SDI Pulse Reject	t _{SPR}	GBD			1.5	µs
SDI Pulse Accept	t _{SPA}	GBD	50			µs
MAGNETIC CARD READER HEAD INPUTS						
Recommended Voltage Level Input	V _{MHI}	(Note 2)	2		200	mV
MCR AFE Current (per Track)	I _{TRACK}	Typical value measured with fixed gain of 3, max value measured with fixed gain of 7		0.6	1.15	mA
FLASH MEMORY						
Write/Erase Cycles			1000			Cycles
Data Retention		T _A = +25°C	100			Years

Note 1: The power-fail reset and power-on-reset detectors operate in tandem so one or both of these signals are active at all times when $V_{DD} < V_{RST}$, ensuring the device maintains the reset state until minimum operating voltage is achieved.

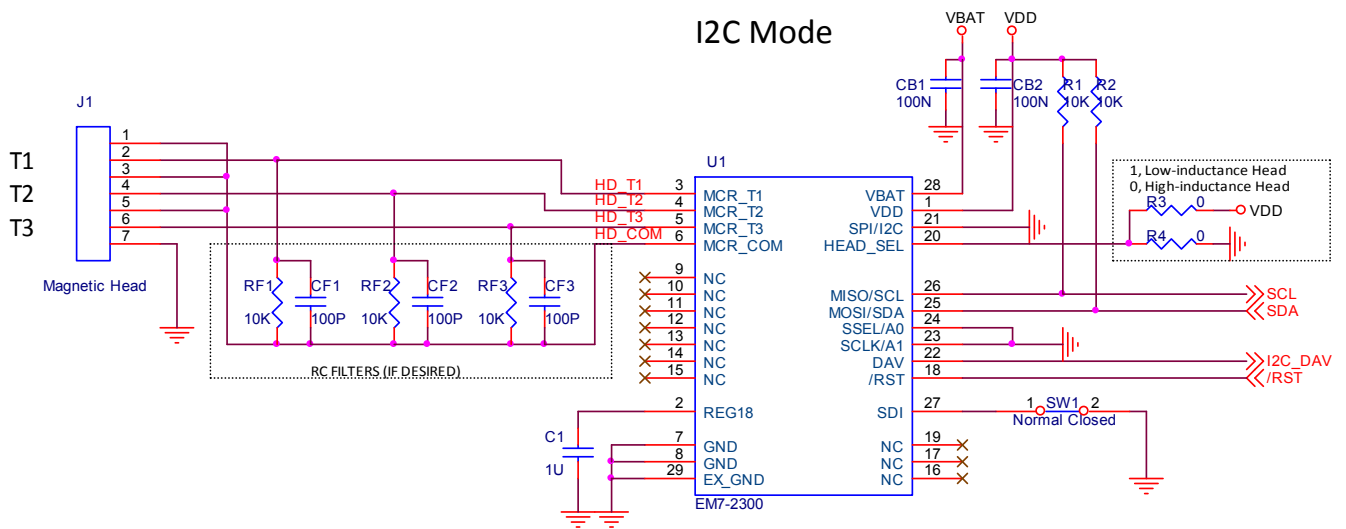
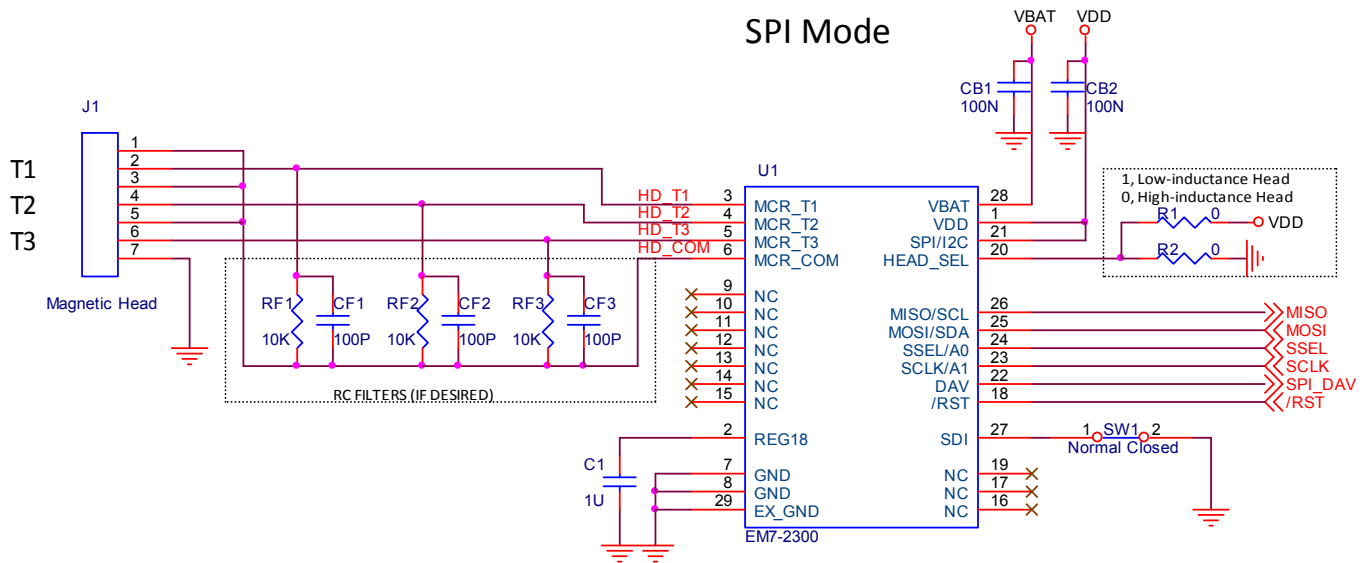
Note 2: Value is the amplitude with a DC offset of MCR_COM output voltage. The 2mV to 200mV is the flux event min/max amplitude from MCR_COM (which is $V_{DD}/2$). The 2mV to 200mV can be above MCR_COM as well as below MCR_COM. The magnetic card reader tolerates as much as 20% noise amplitude.



EM7-2300

Secure Magnetic Card Reader IC

Typical Application Circuit:



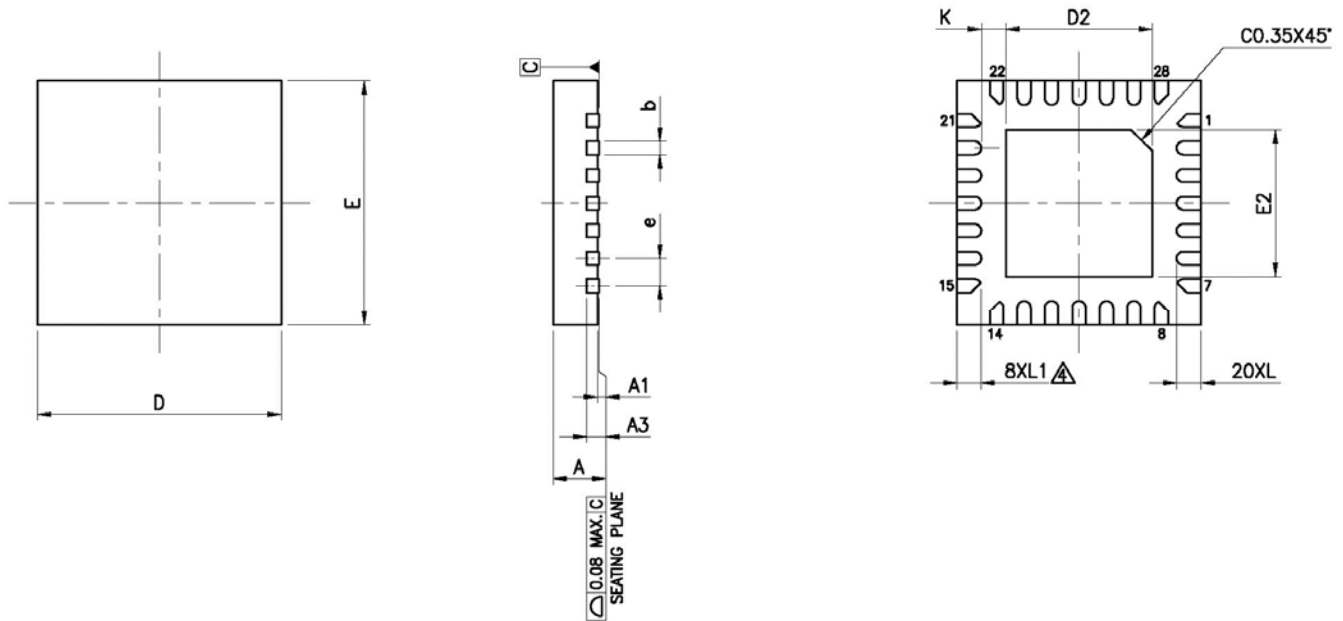
	Inductance Value	HEAD_SEL	RF(1/2/3)	CF(1/2/3)
Low inductance	20mH ~ 60mH	1	3.6kΩ	100pF
High inductance	80mH ~ 140mH	0	10kΩ	100pF



EM7-2300

Secure Magnetic Card Reader IC

Package outline: QFN28L 4x4x0.75mm, pitch 0.45mm



JEDEC OUTLINE	PACKAGE TYPE					
	N/A			N/A		
PKG CODE	WQFN(X428)			VQFN(Y428)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.20 REF.			0.20 REF.		
b	0.17	0.22	0.27	0.17	0.22	0.27
D	4.00 BSC			4.00 BSC		
E	4.00 BSC			4.00 BSC		
e	0.45 BSC			0.45 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
⚠ L1	0.33	0.38	0.43	0.33	0.38	0.43
K	0.20	—	—	0.20	—	—

PAD SIZE	E2			D2			LEAD FINISH	
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF
114X114 MIL	2.30	2.40	2.45	2.30	2.40	2.45	V	X

MSL Rating: Level 3

MSL Standard: IPC/JEDEC J-STD-020

Packing Standard: IPC/JEDEC J-STD-033

ESD Testing:

ESD Standard: JESD22-A114

Human Body Model: 2KV passed

EM7-2300

Secure Magnetic Card Reader IC

Appendix A

I²C Serial Peripheral Specifications

(See Figure 1 and Figure 2.)

PARAMETER	SYMBOL	CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
Input Low Voltage	V_{IL_I2C}	Supply voltages that mismatch I ² C bus levels must relate input levels to the R _P pullup voltage	-0.5	0.3 x V _{DD}	-0.5	0.3 x V _{DD}	V
Input High Voltage	V_{IH_I2C}	Supply voltages that mismatch I ² C bus levels must relate input levels to the R _P pullup voltage	0.7 x V _{DD}		0.7 x V _{DD}	V _{DD} + 0.5V	V
Input Hysteresis (Schmitt)	V_{IHYS_I2C}	V _{DD} > 2V			0.05 x V _{DD}		V
Output Logic-Low (Open Drain or Open Collector)	V_{OL_I2C}	V _{DD} > 2V, 3mA sink current	0	0.4	0	0.4	V
Capacitive Load for Each Bus Line	C _B		400		400		pF
Output Fall Time from V _{IH_MIN} to V _{IL_MAX} with Bus Capacitance from 10pF to 400pF	t _{OF_I2C}	t _{R/F_I2C} exceeds t _{OF_I2C} , which permits RS to be connected as shown in figure	250		20 + 0.1C _B	250	ns
Pulse Width of Spike Filtering That Must Be Suppressed by Input Filter	t _{SP_I2C}				0	50	ns
Input Current on I/O	I _{IN_I2C}	Input voltage from 0.1 x V _{DD} to 0.9 x V _{DD}	-10	+10	-10	+10	μA
I/O Capacitance	C _{IO_I2C}		10		10		pF
I ² C Bus Operating Frequency	f _{I2C}		0	100	0	400	kHz
System Frequency	f _{SYS}		0.90		3.60		MHz
I ² C Bit Rate	f _{I2C}		f _{SYS} /8		f _{SYS} /8		Hz
Hold Time After (Repeated) START	t _{HD:STA}		4.0		0.6		μs
Clock Low Period	t _{LOW_I2C}		4.7		1.3		μs
Clock High Period	t _{HIGH_I2C}		4.0		0.6		μs
Setup Time for Repeated START	t _{SU:STA}		4.7		0.6		μs

EM7-2300

Secure Magnetic Card Reader IC

I²C Serial Peripheral Specifications (continued)

(See Figure 1 and Figure 2.)

PARAMETER	SYMBOL	CONDITIONS	STANDARD MODE		FAST MODE		UNITS
			MIN	MAX	MIN	MAX	
Hold Time for Data	t _{HD:DAT}	A device must internally provide a hold time of at least 300ns for V _{IH_I2C(MIN)} to bridge the undefined region of the falling edge of SCL. The maximum t _{HD:DAT} needs to be met only if the device does not stretch the SCL low period	0	3.45	0	0.9	μs
Setup Time for Data	t _{SU:DAT}	A fast-mode I ² C bus device can be used in a standard-mode I ² C bus system; if such a device does not stretch the low period of the SCL signal, it must output the next data bit to the SDA line t _{R_I2C(MAX)} + t _{SU:DAT} = 1000 + 250 = 1250ns (according to the standard-mode I ² C specification) before the SCL line is released	250		100		ns
SDA/SCL Fall Time	t _{F_I2C}			300	20 + 0.1C _B	300	ns
SDA/SCL Rise Time	t _{R_I2C}			1000	20 + 0.1C _B	300	ns
Setup Time for STOP	t _{SU:STO}		4.0		0.6		μs
Bus Free Time Between STOP and START	t _{BUF}		4.7		1.3		μs
Noise Margin at the Low Level for Each Connected Device (Including Hysteresis)	V _{nL_I2C}		0.1 x V _{DD}		0.1 x V _{DD}		V
Noise Margin at the High Level for Each Connected Device (Including Hysteresis)	V _{nH_I2C}		0.2 x V _{DD}		0.2 x V _{DD}		V

EM7-2300

Secure Magnetic Card Reader IC

I²C Serial Diagrams

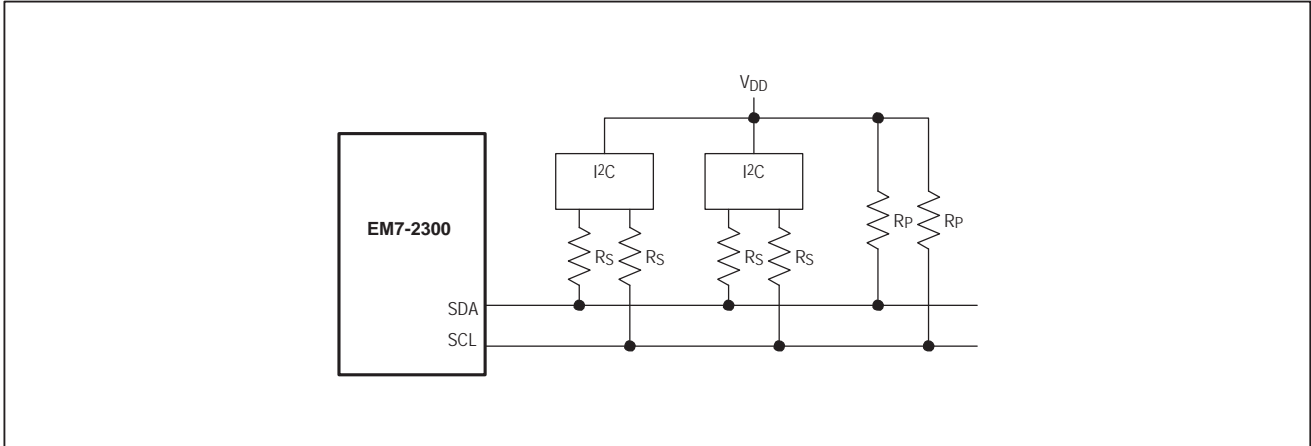


Figure 1. Series Resistors (R_S) for Protecting Against High-Voltage Spikes

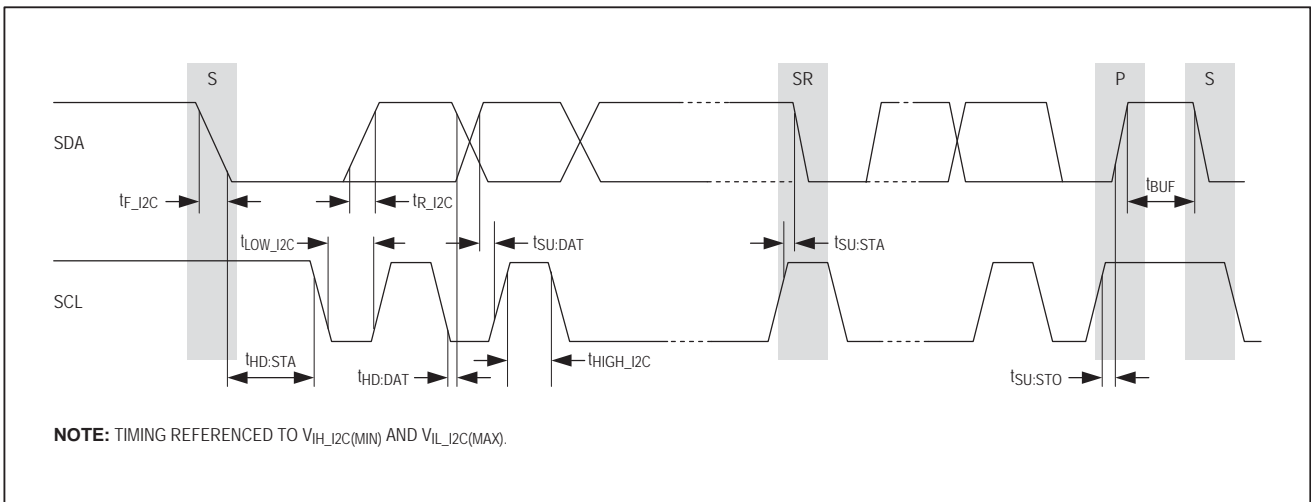


Figure 2. I²C Bus Controller Timing Diagram



EM7-2300

Secure Magnetic Card Reader IC

Serial Peripheral Interface (SPI) Specifications

(See Figure 3 and Figure 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI Master Operating Frequency	$1/t_{MCK}$				$f_{CK}/2$	MHz
SPI Slave Operating Frequency	$1/t_{SCK}$				$f_{CK}/4$	MHz
SCLK Output Pulse-Width High/Low	t_{MCH} , t_{MCL}		$t_{MCK}/2$ - 35			ns
MOSI Output Hold Time After SCLK Sample Edge	t_{MOH}		$t_{MCK}/2$ - 35			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$ - 35			ns
MISO Input Valid to SCLK Sample Edge Rise/Fall Setup	t_{MIS}		35			ns
MISO Input to SCLK Sample Edge Rise/Fall Hold	t_{MIH}		0			ns
SCLK Input Pulse-Width High/Low	t_{SCH} , t_{SCL}			$t_{SCK}/2$		ns
SSEL Active to First Shift Edge	t_{SSE}			50		ns
MOSI Input to SCLK Sample Edge Rise/Fall Setup	t_{SIS}		35			ns
MOSI Input from SCLK Sample Edge Transition Hold	t_{SIH}		35			ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}				70	ns
SCLK Inactive to SSEL Rising	t_{SD}		35			ns

EM7-2300

Secure Magnetic Card Reader IC

SPI Timing Diagrams

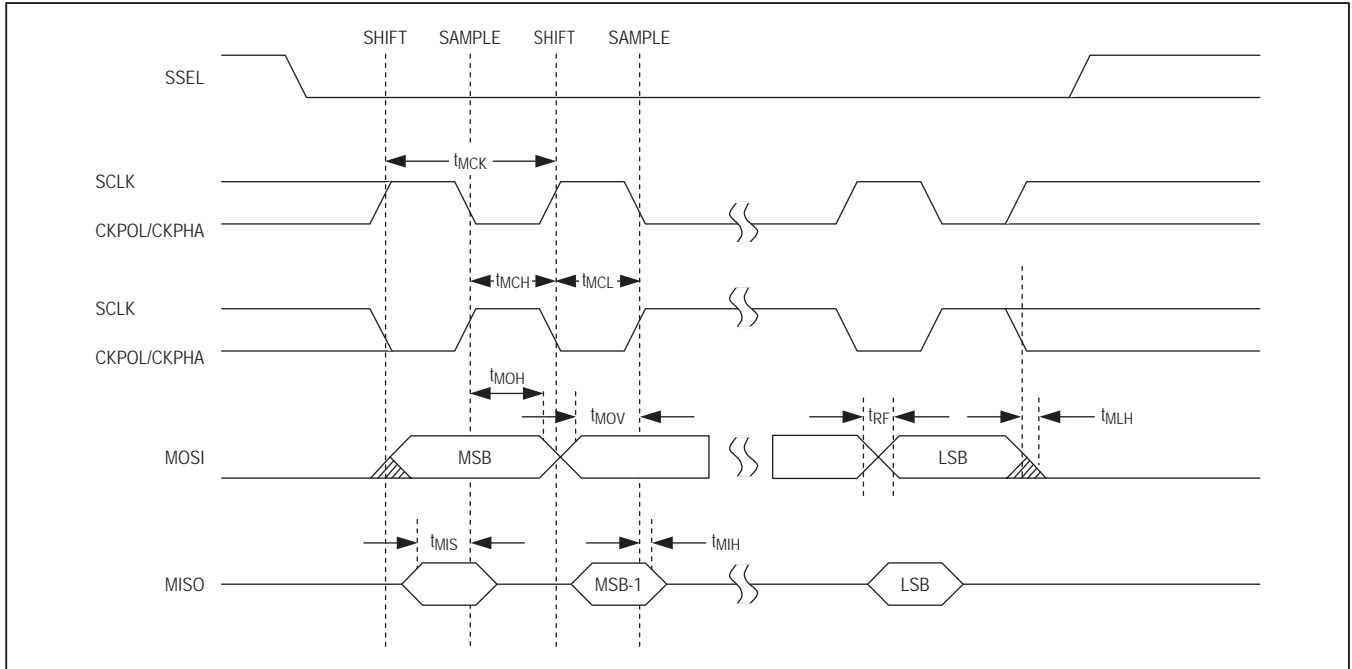


Figure 3. SPI Master Communication Timing

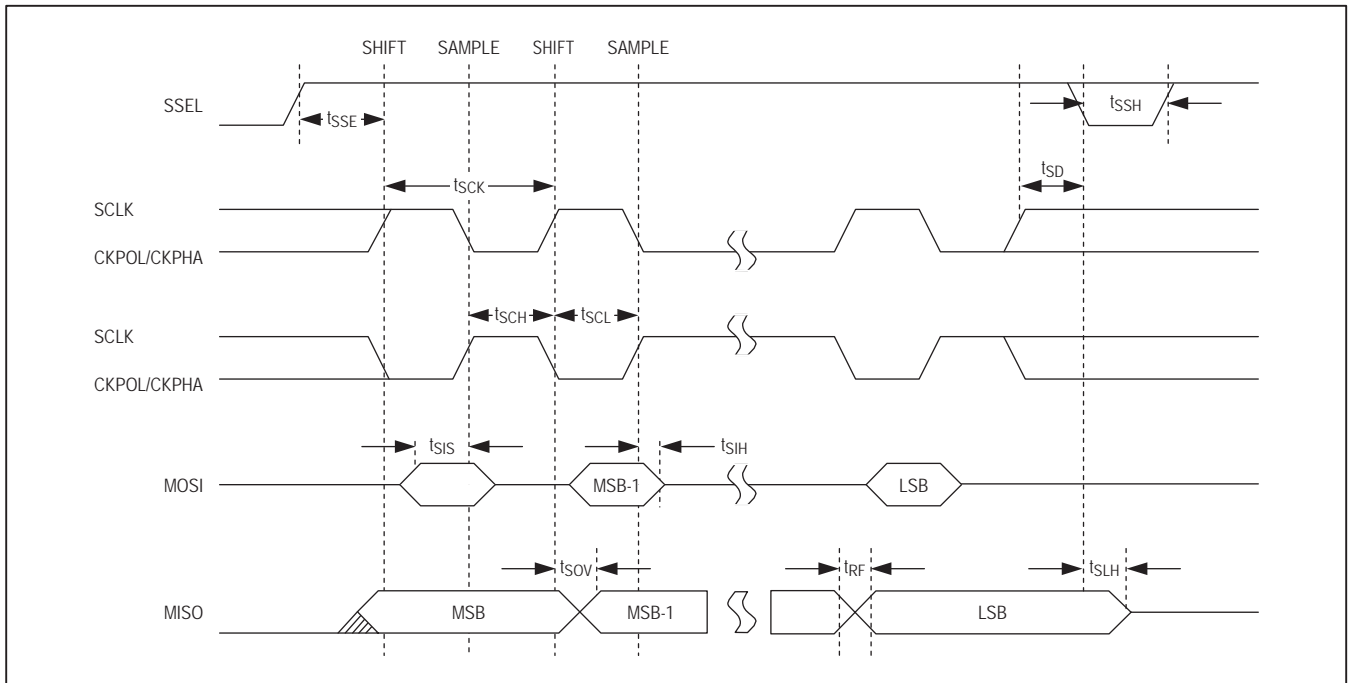


Figure 4. SPI Slave Communication Timing



EM7-2300

Secure Magnetic Card Reader IC

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	05 Dec/2016	First creation.