



M4-2200

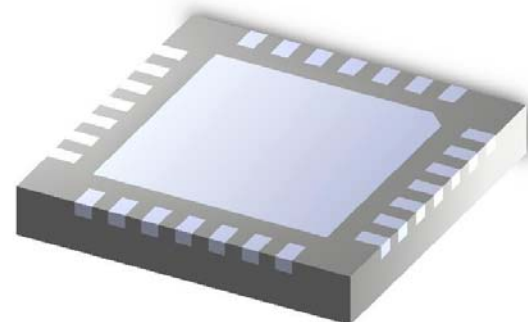
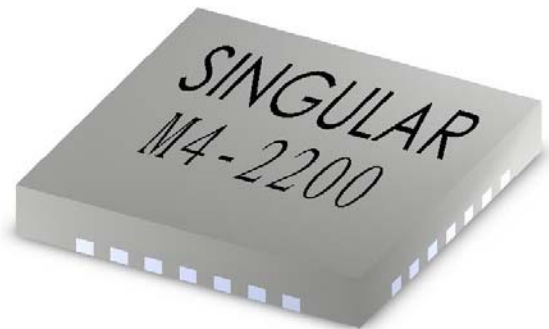
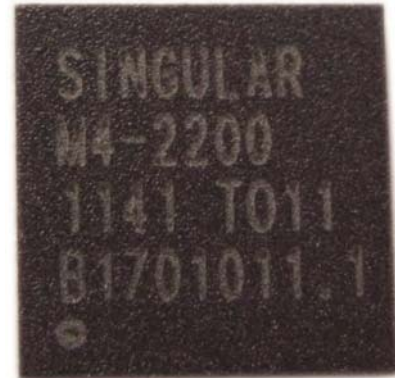
Dual Track F/2F Decoder

signal conditioning and detection block.

Feature

- Fully compatible with M3-2200L or M3-2200G
- Dual track F/2F decoder
- Data processing rate: 300 ~ 15,000 bps per track
- Lower power requirement: DC 5.0 V
Acceptable amplitude from 10% to 200% of ISO reference voltage (i.e. reference signal amplitude)
- CMOS machining
- RoHS compliant, halogen-free mold compound, JEDEC Pb-Free category e3 compliant (100%Sn solder plating), and 260 °C IR reflow test pass

Package



Description

The **M4-2200** F/2F decoder integrated circuit is designed for use in magnetic strip card reader system.

The F/2F read/decoder IC will recover clock and data signals from an F/2F data stream generated from a magnetic head. **M4-2200** will function for data rates from 200 to 15,000 bits per second. Acquisition and tracking of the data within this range is automatically.

M4-2200 is consisted by two major blocks at each channel:

Amplify block-

This block amplifies and filters the signal read from the magnetic reader head, rejects common mode noise and detects signal peaks. It also includes protection circuit to protect the component.

And latches onto the data rate and performs the recovery of individual bits from the F/2F data stream.

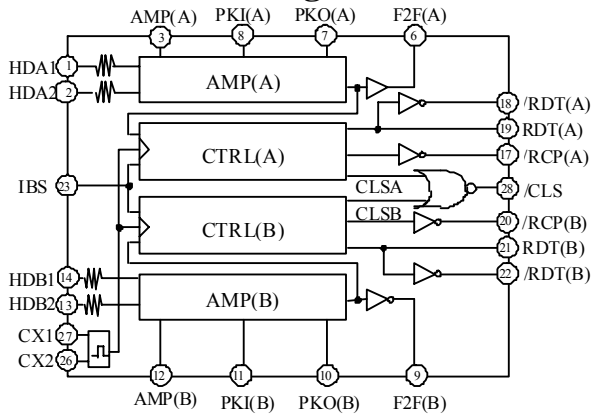
Control block-

The enable and disable counters provide initialization for the recovery block. These counters initialize both bit recovery and the

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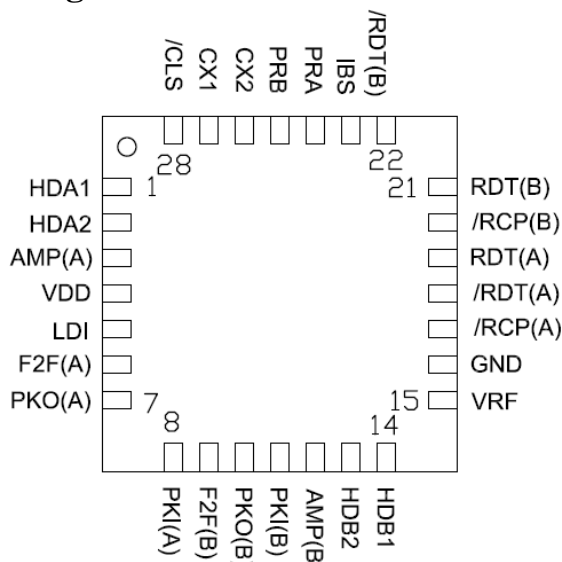
Functional block diagram



Pin description

LD1	Read control
F2F (A/B)	F2F output
PKO (A/B)	Peak detector output
PKI (A/B)	Peak detector input
AMP (A/B)	Amplifier output
HD (A1/2,B1/2)	Amplifier input
VRF	Reference voltage output
GND	Ground
/RCP (A/B)	Read clock output
/RDT (A/B)	Read data output
IBS	Ignore bit select
CX1	Capacitance for oscillation
CX2	Capacitance for oscillation
/CLS	Card loading signal output
Vcc	Power supply
PRA	Internal test point
PRB	Internal test point

Pin assignment

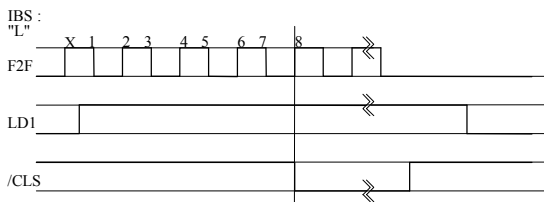
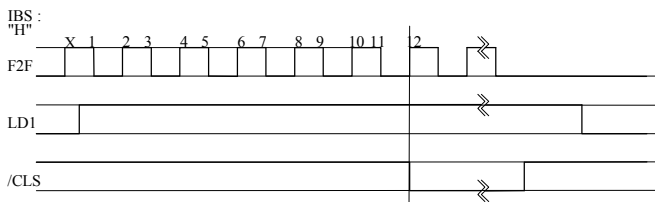


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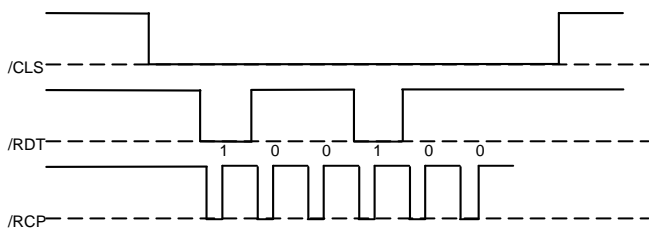
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Setting and timing of ignore bits by IBS

IBS	Number of Ignore bits
L	8
H	12
Description	
<ul style="list-style-type: none"> •“L” of LDI input resets internal digital circuit. •LDI input may be always “H”. •CLS output goes “L” after counting the flux changes FC (F/2F status change) of the number of ignored bits, and goes back “H” when bit internal counter is in full count state. 	

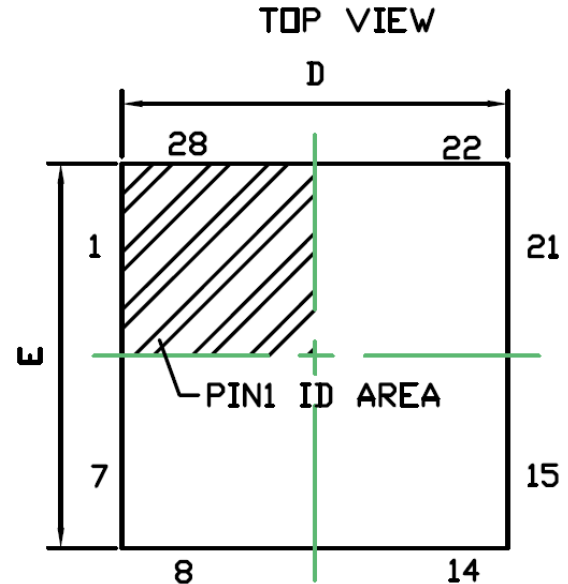


Timing



Package outline

Unit: mil (mm)



MSL/ESD Rating

MSL Rating: Level 3,

MSL Standard: IPC/JEDEC J-STD-020

Packing Standard: IPC/JEDEC J-STD-033

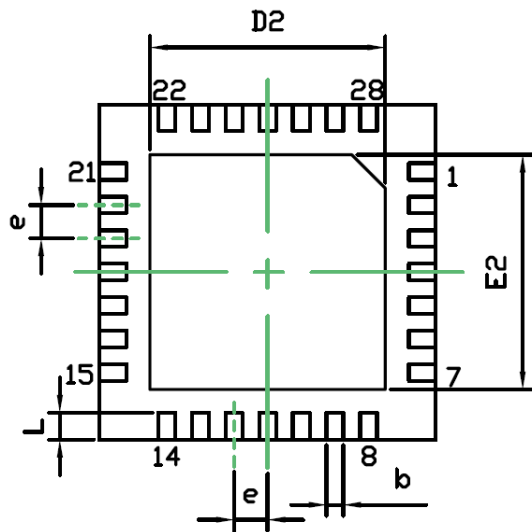
ESD Rating: Class 1B (ESD Sensitive Device!)

Value: Passes between 500 and 999V

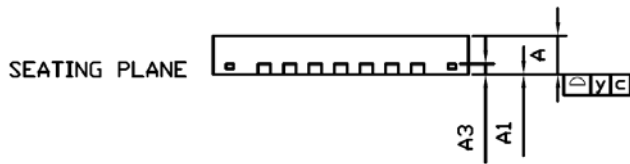
Test: Human Body Model (HBM)

ESD Standard: MIL-STD883G

BOTTOM VIEW



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.203 REF			8.00 REF		
b	0.18	0.25	0.30	7.09	9.84	11.81
D	5.00 BSC			196.85 BSC		
D2	3.40	3.50	3.60	134	138	142
E	5.00 BSC			196.85 BSC		
E2	3.40	3.50	3.60	134	138	142
e	0.50 BSC			19.69 BSC		
L	0.30	0.40	0.50	11.81	15.75	19.69
Y	0.08			3.15		





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Dual Track F/2F Decoder

Electrical characteristics

NO.	Symbol	Parameter	Test Condition	Test ckt.	Min.	Typ.	Max.	Unit
1	V _{REF}	Reference voltage	V _{RF} (A/B)	V _{IN} =0mV _{p-p}	1	—	1.7	V
2	I _{CCW}	Standby circuit current	V _{CC}	V _{IN} =0mV _{p-p}	1	1.8	—	3.5 mA
3	F _{OSC}	Oscillating frequency	/RCP(A/B)	C _{OSC} =33pF	1	—	1	MHz
4	V _{OH}	“H” Output t voltage	/RDT(A/B), /RCP(A/B)	V _{CC} =5V, I _{OH} =-1mA	2	—	4.8	V
5	GV ₁	Voltage gain 1 of OP amp	AMP(A/B)	V _{IN} =50mV _{p-p} , F _{IN} =1KHz, Sine wave	3	—	10	V/V
6	GV ₂	Voltage gain 2 of OP amp	AMP(A/B)	V _{IN} =50mV _{p-p} , F _{IN} =15KHz, Sine wave	3	—	10	V/V
7	V _{OPP}	Maximum output voltage of amp	AMP(A/B)	F _{IN} =1KHz, Sine wave	3	—	3.4	V
8	V _{TH+1}	Positive threshold voltage	PKI(A/B)~ F2F(A/B)		4	—	0.3	V
9	V _{TH-1}	Negative threshold voltage	PKI(A/B)~ F2F(A/B)		4	—	-0.3	V
10	V _{OL2}	“L” Output voltage of F2F	F2F(A/B)	V _{PKI} =0V, I _{F2F} =0.5mA	4	—	57	mV
11	V _{OH2}	“H” Output voltage of F2F	F2F(A/B)	V _{PKI} =5V, I _{F2F} =-0.5mA	4	—	3.1	V
12	I _{OH}	“H” Output current	RDT(A/B)	V _{CC} =5V, V _{OH} =2.4V	5	—	22.6	mA
13			/RCP(A/B), /RDT(A/B)		—	—	-8	—
14	I _{OL}	“L” Output current	RDT(A/B)	V _{CC} =5V, V _{OL} =0.4V	5	—	6.6	mA
15			/RCP(A/B), /RDT(A/B)		5	—	-8.5	—
16	I _{OS}	Output short current	/RCP(A/B), /RDT(A/B)	V _{CC} =5V	5	—	-9	mA
17	T _R	Rise time	/RCP(A/B)	f=1KHz, V _{DC} =0V, V _{p-p} =5V	6	—	30	ns
18	T _F	Fall time	/RCP(A/B)	f=1KHz, V _{DE} =0V, V _{p-p} =5V	6	—	5.7	ns

T_A=25°C, V_{CC}=5V

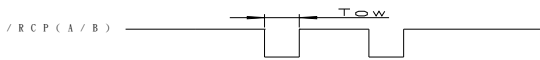
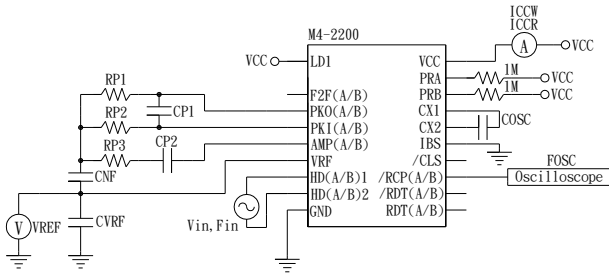
Condition : V_{CC}=5V, C_{OSC}=33 pF, R_{P1}=4.7M, R_{P2}=10K, R_{P3}=1K, C_{P1}=47P, C_{P2}=2200P, C_{NF}=150P, C_{VREF}=0.1U

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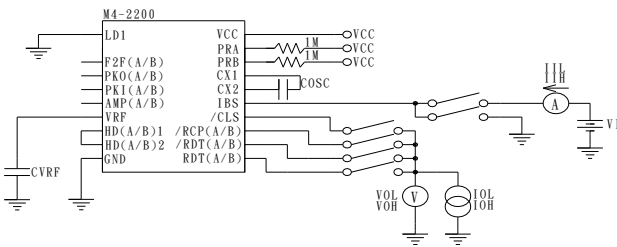
Test Circuits

1. Measurement of VREF, ICCW, ICCR, FOSC



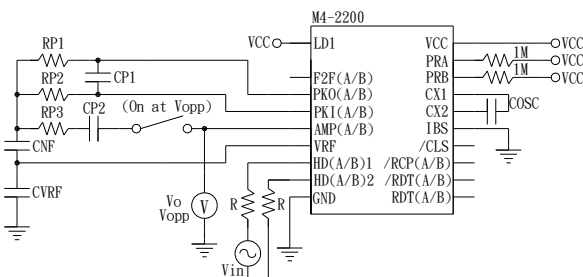
Note: At Cosc = 33p the Tow = 35μs~39μs

2. Measurement of VOL, VOH, IIL, IIH



Note: Short IBS to GND when it is not measured.

3. Measurement of GV1, GV2, RIN, Vopp



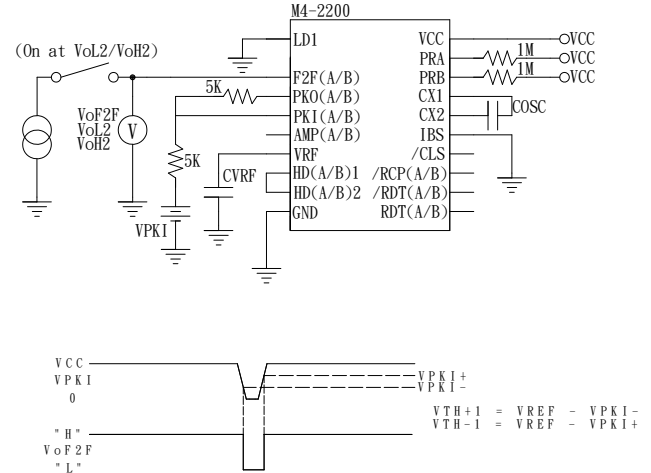
$$GV_1 = \frac{V_o}{V_{in}}$$

$$R_{IN} = \frac{2V_o}{GV_1 \cdot V_{in} - V_o} \cdot R$$

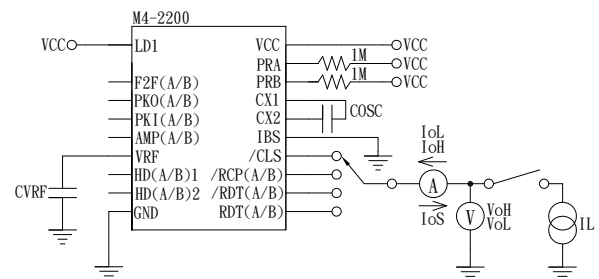
Note: R=0KΩ at measuring GV,
R=10KΩ at measuring RIN

4. Measurement of VTH+1, VTH-1, VOL2, VOH2

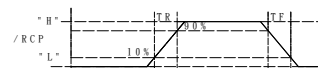
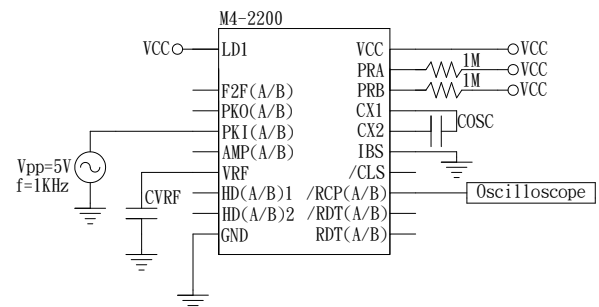
4. Measurement of VTH+1, VTH-1, VOL2, VOH2



5. Measurement of IOH, IOL, IOS



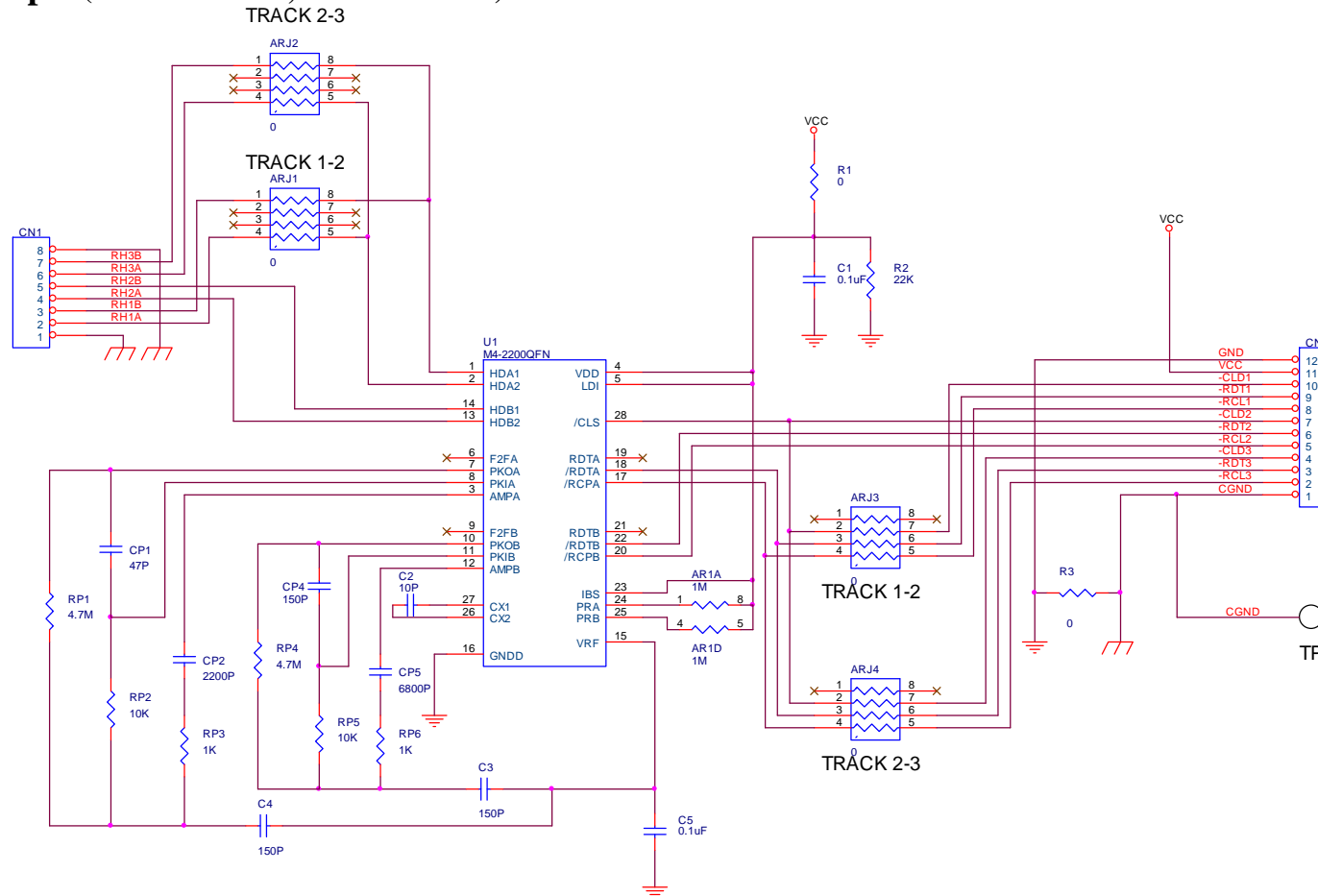
6. Measurement of Tr, Tf



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ISO application example ($V_{CC} = 5.0V$ DC, tolerance $\pm 5\%$)



Note1. We recommend that R2 should be 10K~100K to increase circuit reliability and R2 circuit line should be short.

Note2. If your application must read Track2 with both bit density 75 BPI (ISO) and 210 BPI (non-ISO), you can adjust CP4 to 68P and CP5 to 4700P. The reader's performance usually gets worse than the original one for only reading 75 BPI (ISO).