



M3-2300LQG

Triple Track F/2F Decoder

Feature

- Triple track F/2F decoder
- Data processing rate: 300 ~ 15,000 bps per track
- Lower Power requirement: DC5V
- Acceptable amplitude from 10% to 200% of ISO reference voltage
- CMOS machining
- RoHS compliant, halogen-free mold compound, JEDEC Pb-Free category e6 compliant (98%Sn + 2%Bi solder plating), and 260°C IR reflow test pass



Description

The **M3-2300LQG** F/2F decoder integrated circuit is designed for use in magnetic strip card reader system.

The F/2F read/decoder IC will recover clock and data signals from an F/2F data stream generated from a magnetic head. **M3-2300LQG** will function for data rates from 200 to 15,000 bits per second. Acquisition and tracking of the data within this range is automatically.

M3-2300LQG is consisted by two major blocks at each channel.

Amplify block-

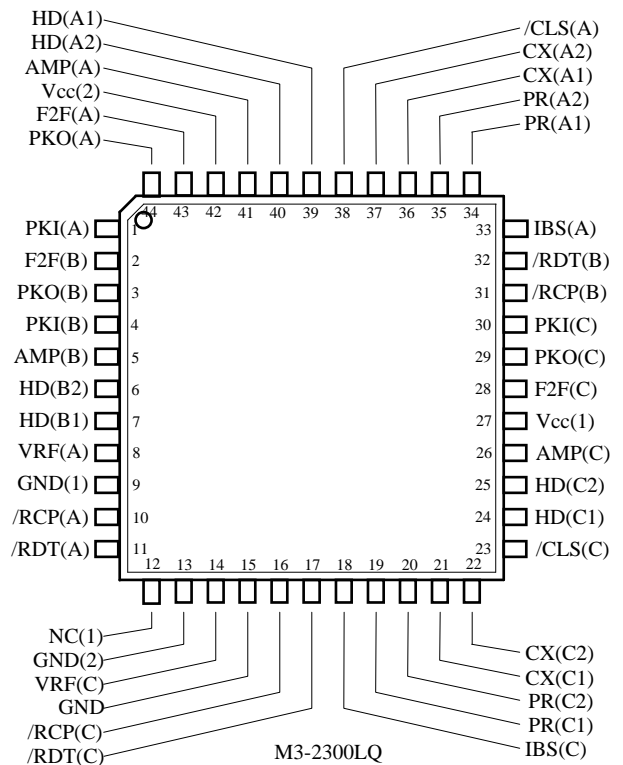
This block amplifies and filters the signal read from the magnetic reader head, rejects common mode noise and detects signal peaks. It also includes protection circuit to protect the component.

And latches onto the data rate and performs the recovery of individual bits from the F/2F data stream.

Control block-

The enable and disable counters provide initialization for the recovery block. These counters initialize both bit recovery and the signal conditioning and detection block.

Pin assignment





Pin description

F2F(A/B/C)	Internal test point
PKO(A/B/C)	Peak detector output
PKI(A/B/C)	Peak detector input
AMP(A/B/C)	Amplifier output
HD(A1/2,B1/2,C1/2)	Amplifier input
VRF(A/C)	Reference voltage output
GND,GND(1/2)	Ground
IBS(A/C)	Ignore bit select
/CLS(A/C)	Card loading signal output
/RDT(A/B/C)	Read data output
/RCP(A/B/C)	Read clock output
CX(A1/C1)	Capacitance for oscillation
CX(A2/C2)	Capacitance for oscillation
PR(A1/C1)	Internal test point
PR(A2/C2)	Internal test point
Vcc(1/2)	Power supply
NC(1)	Non connect