

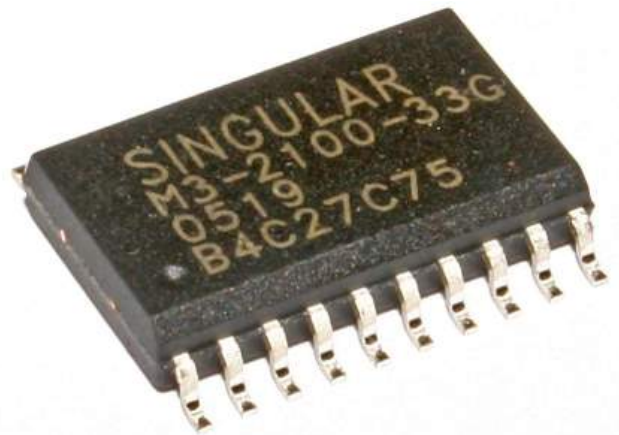


# M3-2100-33G

## Single Track F/2F Decoder

### Feature

- Single track F/2F decoder
- Data processing rate: 300 ~ 15,000 bps per track
- Lower power requirement: DC 3.3 ~ 5.0 V
- Acceptable amplitude from 10% to 200% of ISO reference voltage.
- CMOS machining
- RoHS compliant, halogen-free mold compound, JEDEC Pb-Free category e3 compliant (100%Sn solder plating), and 260 °C IR reflow test pass



### Description

The **M3-2100-33G** F/2F decoder integrated circuit is designed for use in magnetic strip card reader system.

The F/2F read/decoder IC will recover clock and data signals from an F/2F data stream generated from a magnetic head. **M3-2100-33G** will function for data rates from 200 to 15,000 bits per second. Acquisition and tracking of the data within this range is automatically.

**M3-2100-33G** is consisted by two major blocks at each channel:

#### Amplify block-

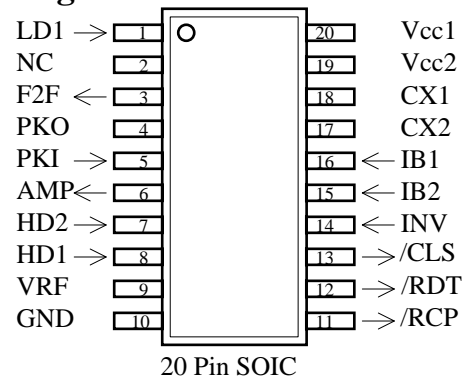
This block amplifies and filters the signal read from the magnetic reader head, rejects common mode noise and detects signal peaks. It also includes protection circuit to protect the component.

And latches onto the data rate and performs the recovery of individual bits from the F/2F data stream.

#### Control block-

The enable and disable counters provide initialization for the recovery block. These counters initialize both bit recovery and the signal conditioning and detection block.

### Pin assignment



### Pin description

LD1	Read control
F2F	F2F output
PKO	Peak detector output
PKI	Peak detector input
AMP	Amplifier output
HD2	Amplifier (-) input
HD1	Amplifier (+) input
VRF	Reference voltage output
GND	Ground
/RCP	Read clock output
/RDT	Read data output
/CLS	Card loading signal output
INV	Inverting input
IB2	Ignore bit 2
IB1	Ignore bit 1
CX2	Capacitance for oscillation
CX1	Capacitance for oscillation
Vcc2	Power supply
Vcc1	Power supply