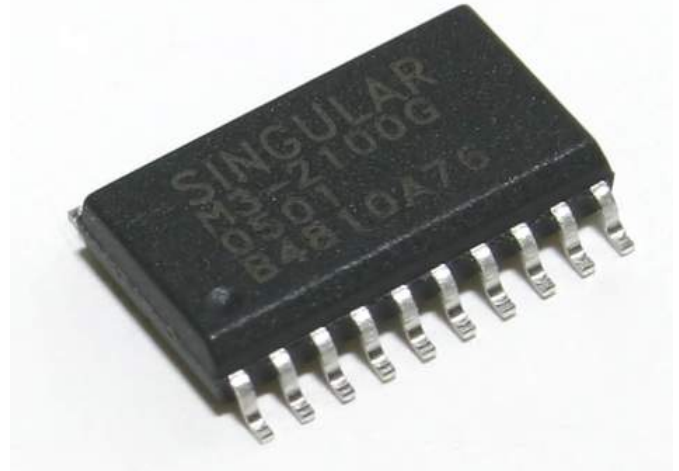


M3-2100G

Single Track F/2F Decoder

Feature

- Single track F/2F decoder
- Data processing rate: 300 ~ 15,000 bps per track
- Lower power requirement: DC 3.3 ~ 5.0 V
- Acceptable amplitude from 10% to 200% of ISO reference voltage.
- CMOS machining
- RoHS compliant, halogen-free mold compound, JEDEC Pb-Free category e3 compliant (100%Sn solder plating), and 260 °C IR reflow test pass



Description

The **M3-2100G** F/2F decoder integrated circuit is designed for use in magnetic strip card reader system.

The F/2F read/decoder IC will recover clock and data signals from an F/2F data stream generated from a magnetic head. **M3-2100G** will function for data rates from 300 to 15,000 bits per second. Acquisition and tracking of the data within this range is automatically.

M3-2100G is consisted by two major blocks at each channel:

Amplify block-

This block amplifies and filters the signal read from the magnetic reader head, rejects common mode noise and detects signal peaks. It also includes protection circuit to protect the component.

And latches onto the data rate and performs the recovery of individual bits from the F/2F data stream.

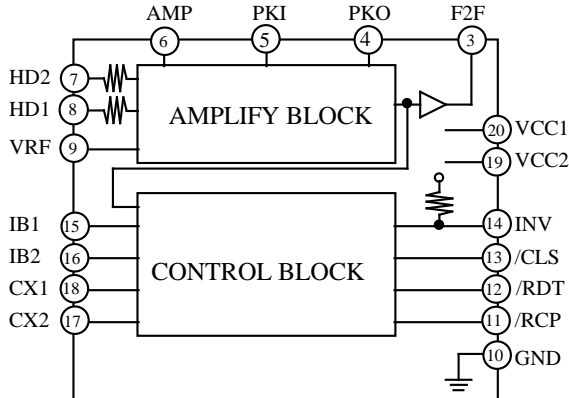
Control block-

The enable and disable counters provide initialization for the recovery block. These counters initialize both bit recovery and the signal conditioning and detection block.

M3-2100G

Single Track F/2F Decoder

Functional block diagram



Setting and timing of ignore bits by IB1/IB2

IB2 input	IB1 input	NO. of Ignore bits
L	L	3
L	H	7
H	L	15
H	H	—

Description

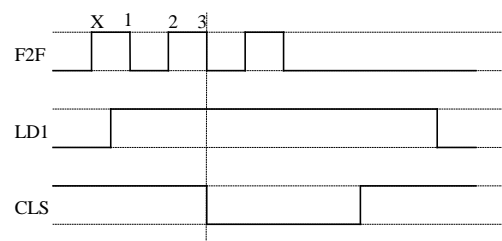
- “L” of LDI input resets internal digital circuit.
- LDI input may be always “H”.
- CLS output goes “L” after counting the flux changes FC(F/2F status change) of the number of ignore bits, and goes back “H” when bit internal counter is in full count state.

Pin description

LD1	Read control
F2F	F2F output
PKO	Peak detector output
PKI	Peak detector input
AMP	Amplifier output
HD2	Amplifier (-) input
HD1	Amplifier (+) input
VRF	Reference voltage output
GND	Ground
/RCP	Read clock output
/RDT	Read data output
/CLS	Card loading signal output
INV	Inverting input
IB2	Ignore bit 2
IB1	Ignore bit 1
CX2	Capacitance for oscillation
CX1	Capacitance for oscillation
Vcc2	Power supply
Vcc1	Power supply

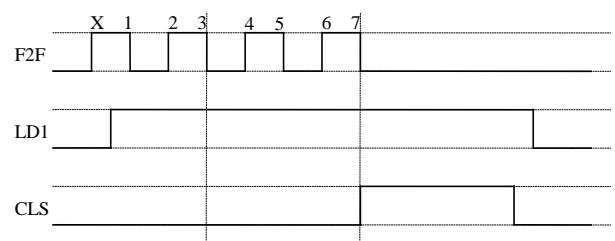
IB2,IB1: "L","L"

INV : "H"

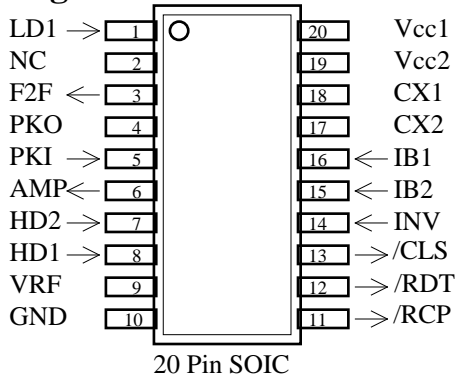


IB2,IB1: "L","H"

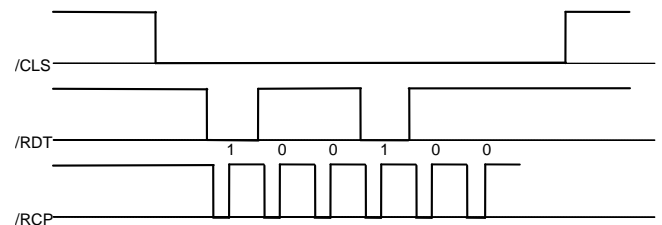
INV : "L"



Pin assignment



Timing

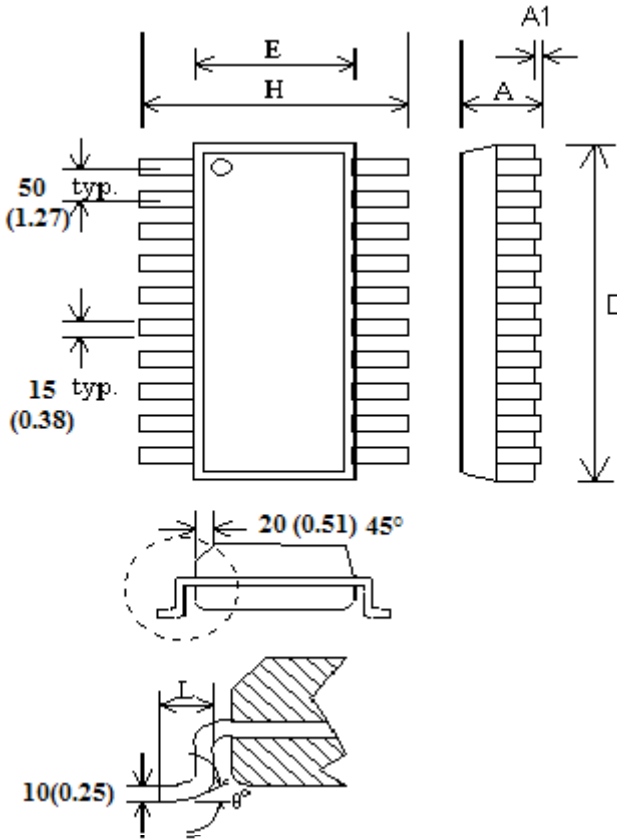




M3-2100G

Single Track F/2F Decoder

Package outline



Unit: mil (mm)

Symbols	Min.	Nom.	Max.
A	94 (2.39)	99 (2.51)	104 (2.64)
A1	4 (0.10)	—	12 (0.30)
D	497 (12.62)	500 (12.7)	510 (12.95)
E	291 (7.39)	295 (7.49)	299 (7.59)
H	394(10.00)	406(10.31)	418(10.62)
L	16 (0.41)	35 (0.89)	50 (1.27)
0°	0°	—	8°

MSL/ESD Rating

MSL Rating: Level 3

MSL Standard: IPC/JEDEC J-STD-020

Packing Standard: IPC/JEDEC J-STD-033

***Must bake @ 125°C 10 hours before SMT.**

Test: HUMAN BODY MODE (HBM)

ESD Standard: MIL-STD-883G

ESD Rating: Class 1B (ESD Sensitive Device!)

Value: Passes between 500 and 999V

Test: MACHINE MODE (MM)

ESD Standard: JEDEC EIA/JESD22-A115

ESD Rating: Class A (ESD Sensitive Device!)

Value: Passes between 50 and 100V



M3-2100G

Single Track F/2F Decoder

Electrical characteristics (1) 5V

NO.	Symbol	Parameter	Test Condition	Test ckt.	Min.	Typ.	Max.	Unit
1	V _{REF}	Reference voltage	V _{REF}	V _{IN} =0mVp-p	1	—	1.7	V
2	I _{CCW}	Standby circuit current	V _{CC1} +V _{CC2}	V _{IN} =0mVp-p	1	1.8	—	3.5 mA
3	F _{OSC}	Oscillating frequency	/RCP	C _{OSC} =33pF	1	—	1	MHz
4	V _{OH}	“H” Output t voltage	/RDT, /RCP	V _{CC} =5V, I _{OH} =-1mA	2	—	4.8	V
5	GV ₁	Voltage gain 1 of OP amp	AMP	V _{IN} =50mVp-p, F _{IN} =1KHz, Sine wave	3	—	10	V/V
6	GV ₂	Voltage gain 2 of OP amp	AMP	V _{IN} =50mVp-p, F _{IN} =15KHz, Sine wave	3	—	10	V/V
7	V _{OPP}	Maximum output voltage of amp	AMP	F _{IN} =1KHz, Sine wave	3	—	3.4	V
8	V _{TH+1}	Positive threshold voltage	PKI~F2F		4	—	0.3	V
9	V _{TH-1}	Negative threshold voltage	PKI~F2F		4	—	-0.3	V
10	V _{OL2}	“L” Output voltage of F2F	F2F	V _{PKI} =0V, I _{F2F} =0.5mA	4	—	57	mV
11	V _{OH2}	“H” Output voltage of F2F	F2F	V _{PKI} =5V, I _{F2F} =-0.5mA	4	—	3.1	V
12	I _{OH}	“H” Output current	RDT	V _{CC} =5V, V _{OH} =2.4V	5	—	22.6	mA
13			/RCP, /RDT		—	-8	mA	
14	I _{OL}	“L” Output current	RDT	V _{CC} =5V, V _{OL} =0.4V	5	—	6.6	mA
15			/RCP, /RDT		5	—	-8.5	mA
16	I _{OS}	Output short current	/RCP, /RDT	V _{CC} =5V	5	—	-9	mA
17	T _R	Rise time	/RCP	f=1KHz, V _{DC} =0V, V _{p-p} =5V	6	—	30	ns
18	T _F	Fall time	/RCP	f=1KHz, V _{DE} =0V, V _{p-p} =5V	6	—	5.7	ns

TA=25°C, V_{CC}=5V

Condition : C_{OSC}=33 pF, RP1=4.7M, RP2=10K, RP3=1K, CP1=47P, CP2=2200P, C_{NF}=150P, C_{VREF}=0.1U

Electrical characteristics (2) 3.3V

NO.	Symbol	Parameter	Test Condition	Test ckt.	Min.	Typ.	Max.	Unit
1	I _{CCW}	Standby circuit current	V _{CC1} +V _{CC2}	V _{IN} =0mVp-p	1	0.75	—	1.5 mA

TA=25°C, V_{CC}=3.3V

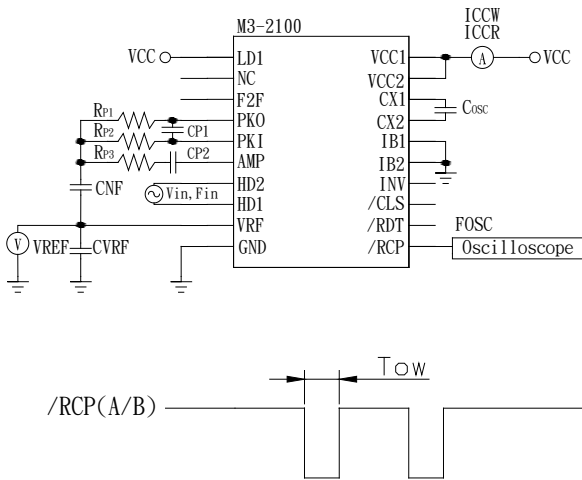
Condition : C_{OSC}=33 pF, RP1=4.7M, RP2=10K, RP3=1K, CP1=47P, CP2=2200P, C_{NF}=150P, C_{VREF}=0.1U

M3-2100G

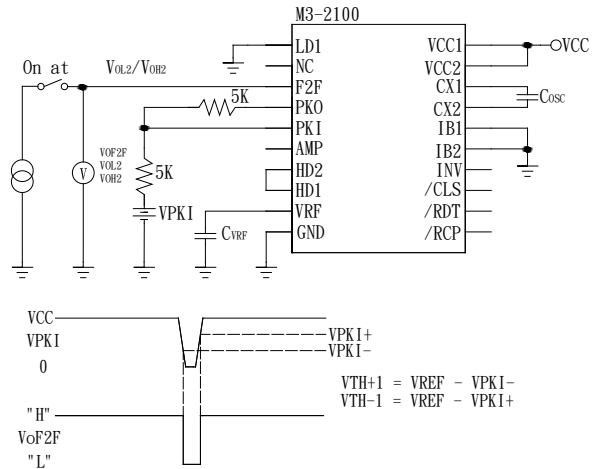
Single Track F/2F Decoder

Test Circuits

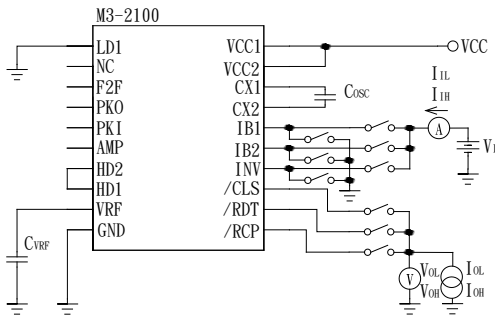
1. Measurement of VREF, ICCW, ICCR, FOSC



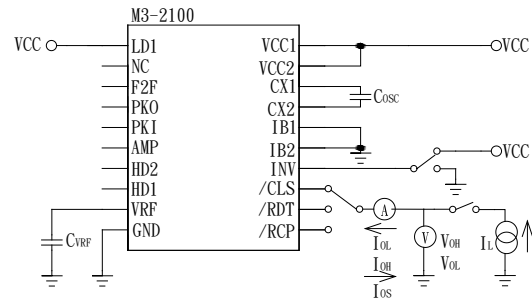
4. Measurement of VTH+1, VTH-1, VOL2, VOH2



2. Measurement of VOL, VOH, IIL, IIH

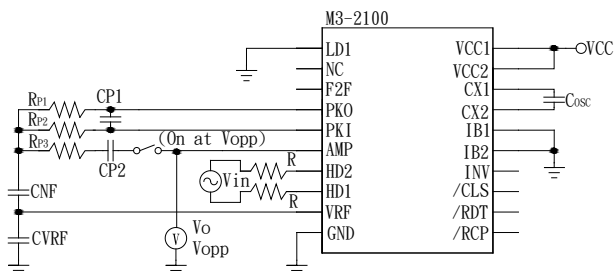


5. Measurement of IOH, IOL, IOS



Note: Short IB1/IB2 to GND when they are not measured.

3. Measurement of GV1, GV2, RIN, Vopp

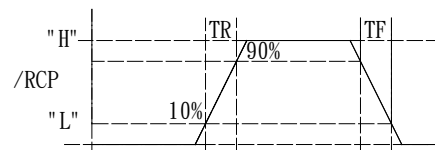
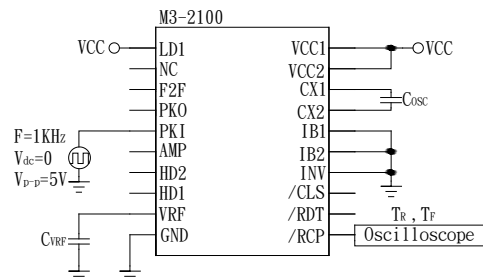


$$GV_1 = \frac{V_o}{V_{in}}$$

$$R_{IN} = \frac{2V_o}{GV_1 \bullet V_{in} - V_o} \bullet R$$

Note: R=0KΩ at measuring GV,
R=10KΩ at measuring RIN

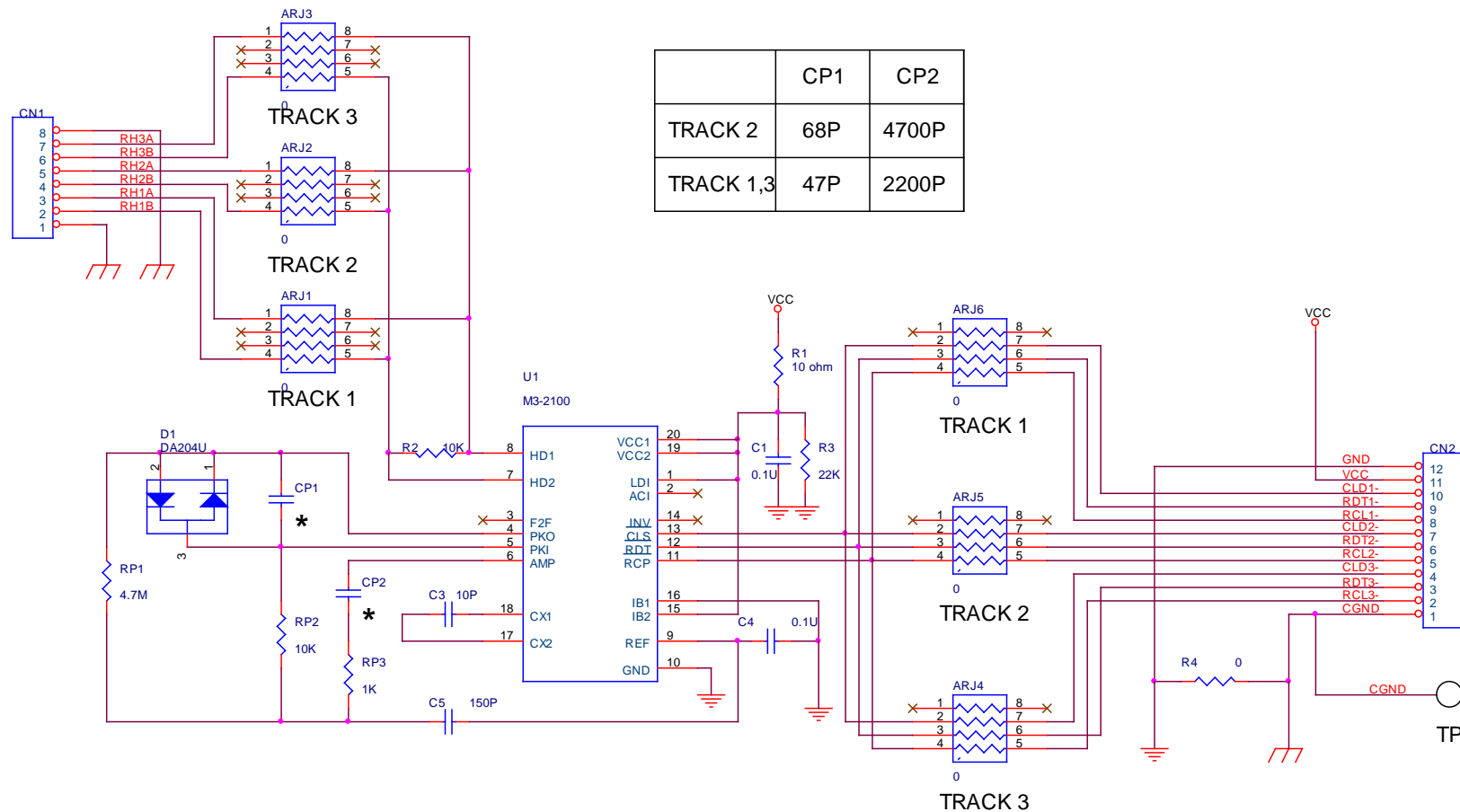
6. Measurement of TR, TF



M3-2100G

Single Track F/2F Decoder

ISO7811 Application Example (VCC = 3.3V DC, tolerance $\pm 5\%$)



Note1. We recommend that R3 should be 10K~100K to increase circuit reliability and R3 circuit line should be short.

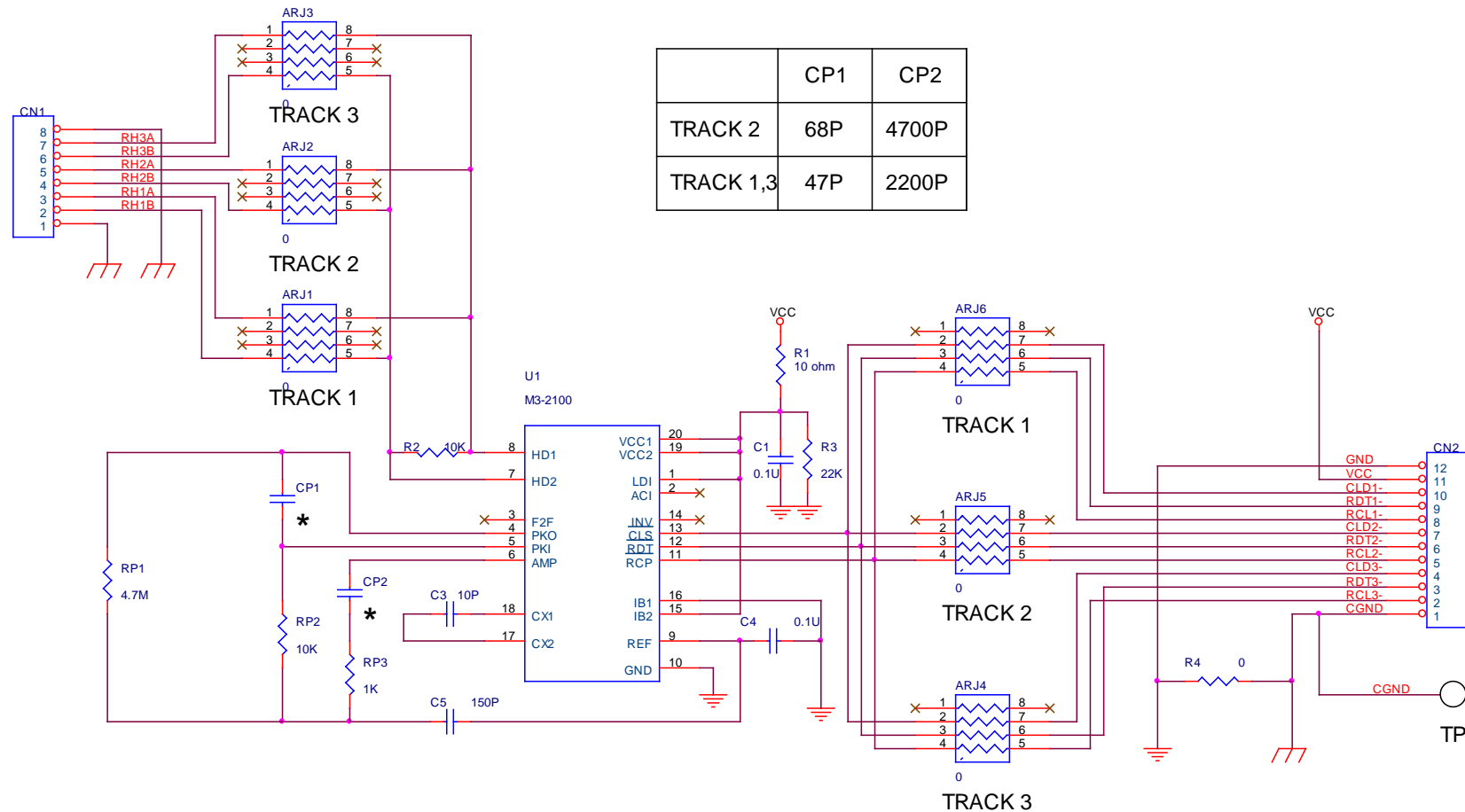
Note2. D1 should be made by Rohm Co., LTD or the ones with the same quality.

Note3. If your application must read Track2 with both bit density 75 BPI (ISO) and 210 BPI (non-ISO), you can adjust CP1 to 68P and CP2 to 4700P. The reader's performance usually gets worse than the original one for only reading 75 BPI (ISO).

M3-2100G

Single Track F/2F Decoder

ISO7811 Application Example (VCC = 5.0V DC, tolerance $\pm 5\%$)



Note1. We recommend that R3 should be 10K~100K to increase circuit reliability and R3 circuit line should be short.

Note2. If your application must read Track2 with both bit density 75 BPI (ISO) and 210 BPI (non-ISO), you can adjust CP1 to 68P and CP2 to 4700P. The reader's performance usually gets worse than the original one for only reading 75 BPI (ISO).